IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	09/751,761
Applicant	:	Ronald D. Smith
Filed	:	December 29, 2000
Title	:	METHOD AND APPARATUS FOR USING NEUTRAL INSTRUCTIONS TO PERFORM ARCHITECTURAL
Group Art Unit	:	2183
Examiner	:	David J. HUISMAN
Customer No.	:	25693

M/S: APPEAL BRIEF – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

REPLY BRIEF

Dear Sir:

This Reply Brief is submitted in response to the Examiner's Answer mailed in this case on August 6, 2007. Due to October 6, 2007 being a Saturday and the PTO being closed on October 8 in observation of the Columbus Day holiday, the present Reply Brief is timely filed.

Appellants submit this Reply Brief to address issues raised in the Examiner's Answer.

REMARKS

Appellants respectfully submit the arguments in the Examiner's Answer are incorrect for at least the following reasons.

Swoboda Does Not Teach Neutral Instructions Being Executed By The Processor To Ascertain An Architectural State Value

In his Answer, the Examiner argues that the processor in Swoboda is executing neutral instructions to obtain an architectural state value because resources are being read "on behalf of the emulation circuitry." Examiner argues that because the read is occurring "on behalf of the emulation circuitry" it is being executed by the processor, but a further reading of Swoboda shows that the read is being executed by a debug-and-test memory access (DT-DMA) mechanism, where the DT-DMA mechanism is configured to operate without direct CPU intervention. *See* Swoboda 26:24-27. Examiner further points to Figures 14 and 15 as showing that the processor executes a neutral instruction to obtain an architectural state value, but Figures 14 and 15 likewise teach "[e]mulation circuitry 851 provides common debug accesses . . . without direct CPU intervention through a [DT-DMA]."

Although Examiner has shown that Swoboda teaches jamming instructions into the instruction register of the processor, Examiner has not shown that those instructions are neutral and has not shown that executing those instructions results in an architectural state value being ascertained. For example, the instruction being jammed might be to force the creation of a hole and halt the execution of further instructions so that the DT-DMA can perform a function. *See e.g.* Swoboda at 26:46-48. Therefore, Examiner has not shown that Swoboda properly teaches certain elements of Appellant's claims.

Swoboda and Ehlig Cannot Be Properly Combined

In his Answer, Examiner makes reference to a portion of Swoboda discussing a multi-processor system and states that it would be obvious to combine the multi-processor system taught in Swoboda with the voting scheme described in Ehlig. Examiner, however, ignores the fact that the systems of Swoboda and Ehlig would be inoperable if combined. Swoboda describes a system that "allows multiple single processor debuggers to be spawned," thus "allow[ing] the user to manipulate each processor individually . . . ." Swoboda 6:7-12. Ehlig, conversely, teaches a system where redundant processors operate in a "lock step" mode where the clocks of the redundant processors are synchronized so that data can be continuously compared. *See e.g.* Ehlig 4:36-40 and 6:17-20. If at any time while the processors are running the data of one processor differs from another processor, then an error signal is output. *Id*. 6:20-22. The advantage of the system described in Ehlig is that data can be continuously compared during real-time operation, and errors can be detected continuously as opposed to only at the conclusion of a particular routine or sub-routine.

Debugging individual processors of a multi-processor system, as taught in Swoboda, is not compatible with a system where the processors are redundant and have synchronized clocks because manipulating a single processor would make that processor asynchronous with the other processors, thus making continuous, real-time comparisons impossible. The system described in Swoboda is, therefore, inoperable if combined with the system described in Ehlig. Thus, the reference cannot be properly combined to support the Examiner's rejections under 35 U.S.C. § 103(a).

Appellants, for at least the reasons described above, have shown that the Examiner's conclusions are in error.

Appellant therefore respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's decision rejecting claims 20-38 and direct the Examiner to pass the case to issue.

The Examiner is hereby authorized to charge any additional fees which may be necessary for consideration of this paper to Kenyon & Kenyon Deposit Account No. 11-0600.

Respectfully submitted,

KENYON & KENYON LLP

Date: October 9, 2007

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